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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,563	09/15/2003	Michael Ryan Davis	200309569-1	9738

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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	**PAPER NUMBER**
2115	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/662,563	DAVIS ET AL.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/8/06 amendments*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 10-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-5 and 10-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 and 10-14 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-5 and 10-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Schelling et al (US Patent 7,036,007[1]; hereinafter Schelling).

4. As per claim 1, Schelling discloses a computer system having a plurality of processors within a cell, the cell comprising:

a processor type register [col. 3, lines 41-43; col. 4, lines 34-36; col. 5, lines 3-7; identifying a processor type],

at least one primary processor [col. 3, lines 37-43; system with multiple primary processors];

a management subprocessor [col. 3, lines 34-37; col. 4, lines 3-7, 26-54; cited columns and lines clearly indicate there is an intelligence that is implemented as a management subprocessor to find, search, and/or locate a processor-specific firmware component(s)];

an EEPROM [col. 7, lines 30-37; flash memory], and

mapping hardware coupling the plurality of processors to the EEPROM [col. 4, line 26 -- col. 5, line 36; col. 7, lines 30-37; mapping via vector location (e.g., address) and entry points];

wherein at system boot the management subprocessor reads the processor type register to determine an appropriate boot image of a plurality of boot images recorded within the EEPROM, and configures the mapping hardware to map the appropriate boot image into boot address space of the at least one primary processors of the cell [col. 3, lines 41-43; col. 4, lines 34-36; col. 5, lines 3-7; identifying a processor type and determining an appropriate processor-specific firmware component(s); col. 4, line 26 -- col. 5, line 36; mapping via vector location (e.g., address) and entry points].

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[1] Prior art cited by the examiner in the prior office action.

5. As per claim 2, Schelling discloses a method of providing firmware to a first processor of a cell of a cellular computer system comprising the steps:

reading information from a processor type register into a management subprocessor [col. 3, lines 41-43; col. 4, lines 34-36; col. 5, lines 3-7; identifying a processor type; col. 3, lines 34-37; col. 4, lines 3-7, 26-54; cited columns and lines clearly indicate there is an intelligence that is implemented as a management subprocessor to find, search, and/or locate a processor-specific firmware component(s)];

determining a processor instruction set architecture from the information read from the processor type register [col. 3, lines 41-43; col. 4, lines 34-36; col. 5, lines 3-7; identifying a processor type];

selecting a compatible boot image from a plurality of boot images, the plurality of boot images contained within an EEPROM of the cell, where each boot image has associated boot-image information, the step of selecting a compatible boot image performed by the management subprocessor [col. 3, lines 41-43; col. 4, lines 34-36; col. 5, lines 3-7; identifying a processor type and determining an appropriate processor-specific firmware component(s)]; and

configuring mapping hardware to map the compatible boot image of the EEPROM into boot address space of the first processor [col. 4, line 26 -- col. 5, line 36; col. 7, lines 30-37; mapping via vector location (e.g., address) and entry points].

6. As per claim 13, Schelling discloses a method of updating firmware on a computer system, the computer system comprising:

at least one processor [col. 3, lines 37-43; multiple processors], and

at least one management processor coupled to a processor type register [col. 3, lines 34-37; col. 4, lines 3-7, 26-54; cited columns and lines clearly indicate there is an intelligence that is implemented as a management processor to find, search, and/or locate a processor-specific firmware component(s)];

the method comprising:

determining a discardable boot image, selected from the group consisting of a boot image incompatible with the processor and a least-recent boot image compatible with the processor [col. 6, lines 43-55; previous version];

erasing the discardable boot image from an EEPROM of the computer system [col. 6, lines 43-55; removing process of the previous version]; and

writing a new boot image to the EEPROM [col. 6, lines 43-55; loading the updated version];

wherein the processor is a processor on a cell of a heterogeneous cellular computer system, the cell comprises the processor coupled through mapping hardware to the EEPROM, and wherein a recent boot image compatible with the processor is retained in the EEPROM when the discardable boot image is erased from the EEPROM [col. 4, line 26 -- col. 5, line 36; col. 7, lines 30-37; mapping via vector location (e.g., address) and entry points; col. 6, lines 43-55]; and

wherein the management processor reads the processor type register at system powerup to determine an appropriate boot image for the processor and the management processor configures the mapping hardware to present said appropriate boot image to the processor [col. 3, lines 34-37; col. 4, lines 3-7, 26-54; cited columns and lines clearly indicate there is an intelligence that is implemented as a management processor to find, search, and/or locate a processor-specific firmware component(s)].

7. As per claim 14, Schelling discloses a method of providing firmware to a first processor of a cell of a cellular computer system comprising the steps:

reading information from a processor type register into a management subprocessor [col. 3, lines 41-43; col. 4, lines 34-36; col. 5, lines 3-7; identifying a processor type; col. 3, lines 34-37; col. 4, lines 3-7, 26-54; cited columns and lines clearly indicate there is an intelligence that is implemented as a management subprocessor to find, search, and/or locate a processor-specific firmware component(s)];

determining a processor instruction set architecture from the information read from the processor type register [col. 3, lines 41-43; col. 4, lines 34-36; col. 5, lines 3-7; identifying a processor type];

selecting a compatible boot image from a plurality of boot images, the plurality of boot images contained within an EEPROM of the cell, where each boot image has associated boot-image information, the step of selecting a compatible boot image being performed by the management subprocessor [col. 3, lines 41-43; col. 4, lines 34-36; col. 5, lines 3-7; identifying a processor type and determining an appropriate processor-specific firmware component(s)]; and

configuring mapping hardware to map the compatible boot image of the EEPROM into boot address space of the first processor [col. 4, line 26 -- col. 5, line 36; col. 7, lines 30-37; mapping via vector location (e.g., address) and entry points];

wherein the boot images include boot images for more than one family of processor instruction set architectures [col. 3, lines 37-43; multiple processors].

8. As per claim 3, Schelling discloses that the step of selecting a compatible boot image is performed by a management subprocessor of the cell [col. 3, lines 34-37; col. 4, lines 3-7, 26-54; cited columns and lines clearly indicate there is an intelligence that is implemented as a management subprocessor to find, search, and/or locate a processor-specific firmware component(s)].

9. As per claims 4 and 5, Schelling discloses that the boot-image information comprises version information [col. 6, lines 48-55].

10. As per claim 10, Schelling discloses that the boot images include for more than one family of processor instruction set architectures [col. 3, lines 37-43].

11. As per claim 11, Schelling discloses that the computer system is a heterogeneous cellular computer system [col. 3, lines 29-43].

12. As per claim 12, Schelling discloses the invention [col. 2, lines 29-34; col. 3, line 29 -- col. 4, line 54; col. 7, lines 31-50; col. 8,lines 13-30].

Response to Arguments

13. Applicant's arguments with respect to claims 1-5 and 10-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.